A Parameter Extraction Technique for Heterojunction Bipolar Transistors

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Abstract

A technique useful for parameter extraction of heterojunction bipolar transistors is presented. The technique makes use of a 'tee' equivalent circuit based upon the physical operation of the device. The technique uses the device f_T, determined by extrapolation of the device h parameters, to establish the total emitter-to-collector delay time from the experimental data. This information is used to establish an equation that is used to constrain the circuit elements, thereby facilitating the parameter extraction procedure. The technique is easily implemented using commercially available computer software.

I. Introduction

Equivalent circuit modeling can provide valuable design information for optimizing the RF performance of solid state devices. In order to maximize the benefits from this approach, however, it is necessary to determine a suitable equivalent circuit topology and accurate element values. To be useful as a design aid the equivalent circuit must have elements that accurately represent physical phenomena known to be important to device performance. Physically based circuits, unfortunately, can be complex with many elements and are, in general, difficult to determine from terminal measurements.

In this paper a technique that has been developed for the parameter extraction of heterojunction bipolar transistors is presented. The technique makes use of a emitter-to-collector delay time equation to constrain the circuit element values in the optimization. In this manner the circuit elements are forced to vary in a manner consistent with the physical operation of the device. The technique is demonstrated by application to state-of-the-art InGaAs/AlInAs/InP HBTs fabricated by Hughes Research Laboratories.

II. Parameter Extraction Technique

As circuit complexity is increased the determination of element values from terminal RF measurements becomes increasingly difficult and, in fact, can become impossible. For example, it is known that unique parameter values cannot be determined solely from RF terminal measurements for circuits with more than a few elements [1]. Many combinations of elements can be found that will result in 'satisfactory' agreement between measured and model produced data. Many of the solutions, however, are non-physical. For this reason, it is desirable to independently determine as many element values as possible from other measurements or calculations. The techniques presented by Fukui [2] for determining parasitic resistances from I-V data and by Curtice [3] for determining parasitic impedances from measured 'cold FET' data, where RF measurements are made with the device biased at zero volts, yield valuable information. In addition, knowledge of bonding pad geometry can be used to determine estimated values for pad capacitances. These techniques allow 'reasonable' element values to be established for some of the elements, thereby providing a starting position for the optimization process used to match model and measured terminal data.

Many elements, however, remain difficult to determine. For example, the delay time associated with the current generator in microwave/mm-wave device equivalent circuits is relatively insensitive to device performance at frequencies at which measured data is generally available (e.g., 0.045-26.5 GHz with a CASCADE Microprober and HP Automatic Network Analyzer). This parameter, however, is very important in determining the high frequency performance of the devices [4]. For example, it has been shown [5] that the phase delay associated with the current generator can lead to high frequency negative conductance in the output and greater than -6 db/octave roll-off of the unilateral gain.

The technique presented in this paper follows the approach stated above and makes use of information provided by the Fukui and Curtice methods. A novel feature of this technique is the linking of delay times associated with the physical operation of the transistor. It is known that the total emitter-collector delay time can be

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defined from the sum of four separate delay times: the base-emitter capacitance charging time (τ_e), the base transit-time (τ_b), the base-collector transit-time (τ_c'), and the base-collector capacitance charging time (τ_c). The total emitter-to-collector delay time can, therefore, be expressed by the equation

$$\tau_{ec} = \tau_e + \tau_b + \tau_c + \tau_c'$$

The base-emitter and base-collector charging times are given by the expression

$$\tau_e, \tau_c = \frac{\left(\frac{a}{C_{be}} + \frac{b}{C_{bc}}\right) \pm \left[\left(\frac{a}{C_{be}} - \frac{b}{C_{bc}}\right)^2 + \frac{4r_b^2}{C_{bc}C_{be}}\right]^{\frac{1}{2}}}{2\left[r_e r_c + r_b r_c + r_b r_e\right]}$$

where

$$a = r_c + r_b + (r_e r_c + r_b r_c + r_b r_e)\, r_{be}$$

and

$$b = r_b + r_e + (r_e r_c + r_b r_c + r_b r_e)\, r_c$$

The emitter-collector delay time can be determined from the measured data by converting the measured S-parameters to h-parameters and projecting h_{21} to unity current gain to determine the device f_T. It can be shown that h_{21} falls at a rate of -6 db/octave, even for circuits of significant complexity, and deviates only at high frequencies. At frequencies near f_T common-lead impedance results in feedback between the output and input circuits and an additional pole is introduced in the characteristic function. This pole, however, has no effect at the frequencies at which the S-parameters are measured (i.e., up to 26.5 GHz).

The sum of the individual delay times is set equal to the emitter-collector delay time as determined from f_T. The resulting equation serves to link and thereby constrain the parameter variables of first order importance. The equation is solved for the base transit-time, since the other delay times are more readily determined. That is, the emitter-base capacitance charging time is determined from C_{be} and R_{be}, and these elements are strong functions of S_{11}. Likewise, the base-collector element values and delay times are strongly affected by S_{22}. Also, elements associated with the current generator are affected by S_{21}. Once these elements are determined the base transit-time is easily determined. This technique is readily implemented using commercially available software. The technique was implemented using TOUCHSTONE and the constrained variable (delay time) equation was formulated using the EQN block within this program.

III. Results

The de-embedded equivalent circuit used in this work is shown in Fig. 1. In order to match the experimental data bonding pad capacitances and lead inductances are added. The circuit results in excellent agreement between measured S-parameters and those determined from the model. For example, the normalized error function defined as the sum of the differences between the measured and model data normalized to the measured data over the frequency range of 0.045-26.5 GHz is less than 1% and typically a few tenths of a percent for the mm-wave transistors used in this work. These GaInAs/AlInAs/InP heterojunction bipolar transistors were fabricated by Hughes Research Laboratories and have f_T's in the range of 20-50 GHz and f_{max}'s in the range of 20-60 GHz. The f_T and f_{max} for a single emitter transistor as a function of collector current is shown in Fig. 2. The f_{max} and f_T peak at about 3 and 5 mA, respectively. Equivalent circuits were determined for these devices at a variety of bias conditions. The base-emitter resistance R_{be} and capacitance C_{be} and the base-collector capacitance C_{bc} are shown in Fig. 3 as a function of collector current for a collector voltage of $V_{ce} = 1.7$ v. The C_{be} increases and the R_{be} decreases with I_{ce} as expected for an increasingly forward biased pn junction. The base-collector capacitance, C_{bc}, obtains a minimum value at a collector current of about 4 mA, and then increases. The increase in C_{bc} is due to charge storage in the undoped collector region due to base push-out (Kirk Effect). The base-emitter resistance R_{be} can be used to calculate the base-emitter junction ideality factor, n, as shown in Fig. 4. The ideality factor varies from a value of about 2 at low collector current to a value of unity at high collector current. This indicates that charge transport across the base-emitter junction is dominated by recombination at low current and thermionic emission at high current.

The delay times determined by this technique for a transistor biased with Vce = 1.70 v are shown in Fig. 5. As indicated, it is possible to explicitly determine the individual delay times, as well as all equivalent circuit parameters. The base delay time is seen to be dominant. The base transit-time is increased and the base-collector transit-time is reduced as a function of collector current due to base push-out and the corresponding decrease in the collector region, in agreement with the determined value for C_{bc}.

IV. Conclusions

A technique useful for the parameter extraction of heterojunction bipolar transistors has been presented. The technique makes use of a delay time equation to constrain the variables used in the optimization procedure. The constraining equation forces the equivalent circuit element values to vary in a manner consistent with the physical operation of the device. The technique is easily implemented using commercially available software. The information provided by this parameter extraction technique yields considerable insight into the physical operation of heterojunction bipolar transistors and provides guidance relative to optimized device design.

References

[1]. R.L. Vaitkus,"Uncertainty in the Values of GaAs MESFET Equivalent Circuit Elements Extracted From Measured Two-Port Scattering Parameters," *Proc. IEEE/Cornell Conf. on High-Speed Semiconductor Devices and Circuits*, 1983, pp. 301-308.

[2] H. Fukui,"Determination of the Basic Device Parameters of a GaAs MESFET," *Bell Sys. Tech. J.*, vol. 58, pp.771-797, Mar. 1979.

[3] W.R. Curtice,"GaAs MESFET Modeling and Nonlinear CAD," *IEEE Trans. Microwave Theory and Tech.*, vol. MTT-36, pp. 220-230, Feb. 1988.

[4] R.J. Trew,"Equivalent Circuits for High Frequency Transistors," *Proc. IEEE/Cornell Conf. on Advanced Concepts in High Speed Semiconductor Devices and Circuits*, 1987, pp. 199-208.

[5] N. Dagli, W. Lee, S. Prasad and C.G. Fonstad,"High-Frequency Characteristics of Inverted-Mode Heterojunction Bipolar Transistors," *IEEE Electron Dev. Lett.*, vol. EDL-8, pp. 472-474, Oct. 1987.

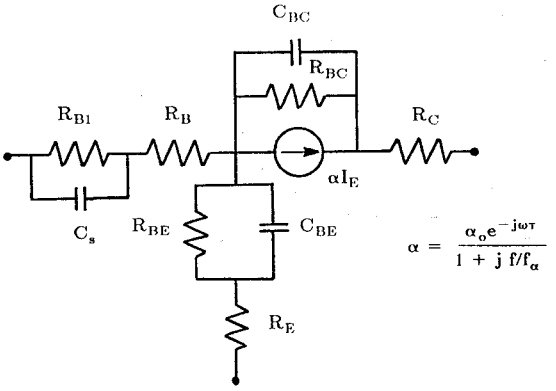

Fig. 1 HBT Equivalent Circuit

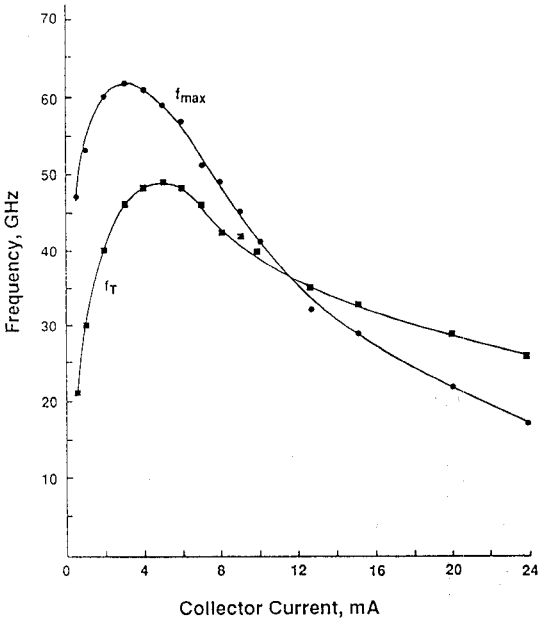

Fig. 2 f_T and f_{max} versus I_{ce} for a Single Emitter HBT

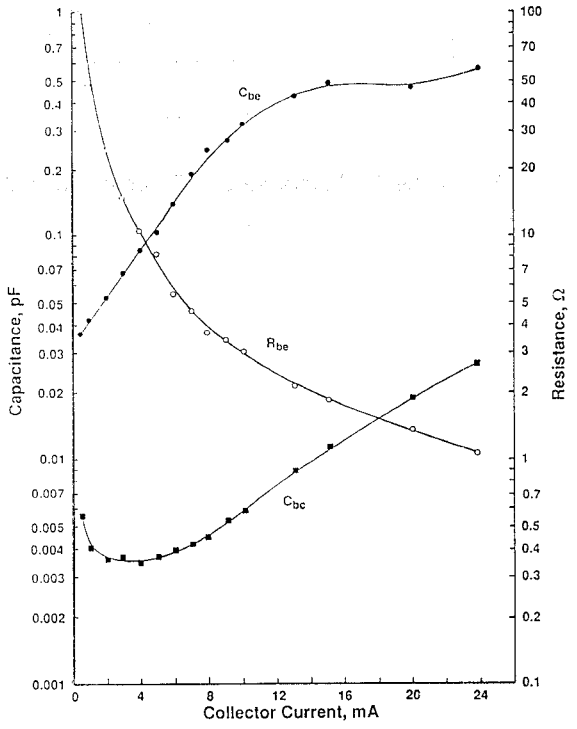

Fig. 3 C_{be}, R_{be} and C_{bc} versus I_{ce} for the HBT

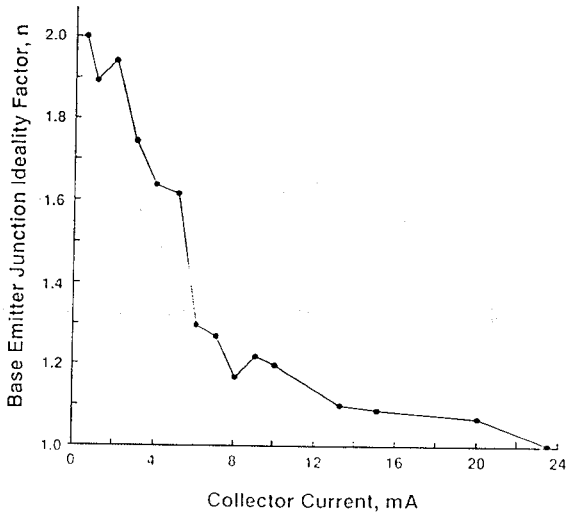

Fig. 4 Ideality Factor versus Collector Current

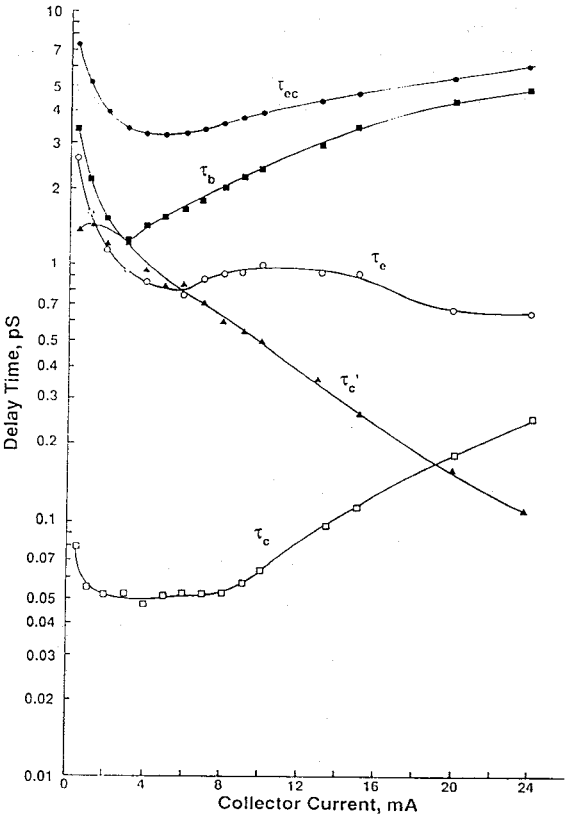

Fig. 5 Delay Times versus Collector Current